

CLAIMS

What is claimed is:

1. A method for adjusting a frequency range of a delay cell of a VCO, the method comprising:

providing a CMOS latch of predetermined gain; and

5 altering transconductance in the CMOS latch to alter a frequency range of the CMOS latch without altering the predetermined gain.

2. The method of claim 1 wherein altering transconductance further comprises coupling at least one pair of series connected transistors in parallel with each switching
10 device of the CMOS latch.

3. The method of claim 2 further comprising coupling a gate of one of the pair to a switching signal node of the CMOS latch and coupling a gate of the other of the pair to a control signal node of the CMOS latch.

15 4. The method of claim 2 wherein each switching device further comprises a transistor.

5. The method of claim 4 wherein the pair of series connected transistors comprise a
20 matching transistor type and a same transistor type as the transistor switching device.

6. A system for adjusting a frequency range of a delay cell of a VCO, the system comprising:

a CMOS latch of predetermined gain; and

means for altering transconductance in the CMOS latch to alter a frequency range of
5 the CMOS latch without altering the predetermined gain.

7. The system of claim 6 wherein the means for altering transconductance further comprises at least one pair of series connected transistors coupled in parallel with each switching device of the CMOS latch.

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8. The system of claim 7 wherein a gate of one of the pair is coupled to a switching signal node of the CMOS latch and a gate of the other of the pair is coupled to a control signal node of the CMOS latch.

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9. The system of claim 7 wherein each switching device further comprises a transistor.

10. The system of claim 9 wherein the pair of series connected transistors comprise a matching transistor type with the transistor.

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11. A delay cell of variable frequency range with substantially constant gain for use in a VCO, the delay cell comprising:

a CMOS latch including a plurality of switching devices; and

at least one path of increased transconductance across each of the plurality of switching devices, wherein the CMOS latch switches faster while maintaining substantially constant gain.

5 12. The delay cell of claim 11 wherein each of the plurality of switching devices further comprises a switching device transistor.

13. The delay cell of claim 12 wherein the at least one path of increased transconductance further comprises at least one pair of transistors connected in series.

10 14. The delay cell of claim 13 wherein one of the at least one pair of transistors comprises a transistor with a gate coupled to a gate of the switching device transistor and another of the at least one pair of transistors comprises a transistor with a gate coupled to a control voltage.

15 15. The delay cell of claim 11 wherein the CMOS latch further comprises a cross-coupled pair of transistors to limit the gain of the CMOS latch.

20 16. The delay cell of claim 13 wherein each of the at least one pair of transistors comprises a matching transistor type to each other and to the switching device transistor.